

WHAT IS CLAIMED IS:

1. A surge protection and reset circuit for a discharge lamp comprising:

a ballast electrically connected to said discharge lamp for igniting said discharge lamp;

5 a starting control circuit electrically connected to said ballast for triggering said ballast to ignite said discharge lamp and powering said ballast;

a microprocessor electrically connected to said starting control circuit for initializing said starting control circuit when said
10 microprocessor receives a lamp-state signal and a reset signal; and

a reset circuit having an output terminal electrically connected to said microprocessor for providing said reset signal to reset said microprocessor when said reset circuit receives said lamp-state signal from a lamp-state terminal of said ballast.

15 2. The surge protection and reset circuit according to claim 1, wherein said surge protection and reset circuit further comprises a first voltage regulator electrically connected to said microprocessor and said starting control circuit for providing a first voltage level to said starting control circuit when said microprocessor outputs a first control signal to said
20 first voltage regulator.

3. The surge protection and reset circuit according to claim 2, wherein said microprocessor outputs said first control signal when said microprocessor receives said lamp-state signal.

4. The surge protection and reset circuit according to claim 1, wherein
25 said microprocessor has a reset terminal electrically connected to said output terminal of said reset circuit.

5. The surge protection and reset circuit according to claim 5, wherein

said reset circuit comprises:

a first transistor having a base terminal electrically connected to one end of a first resistor, and the other end of said first resistor electrically connected to said lamp-state terminal;

5 a second resistor having one end electrically connected to an collector terminal of said first transistor, and the other end of said second resistor being ground; and

at least one first capacitor electrically connected to an emitter terminal of said first transistor and a voltage supply, and the other end of
10 said at least one first capacitor electrically connected to said reset terminal of said microprocessor.

6. The surge protection and reset circuit according to claim 1, wherein said starting control circuit comprises:

a silicon control rectifier (SCR) having a first terminal electrically
15 connected to said output terminal of said first voltage regulator;

a third resistor having one end electrically connected to a second terminal of said silicon control rectifier, and the other end of said third resistor electrically connected to a fourth resistor;

a fifth resistor having one end electrically connected to an
20 intersection of said third resistor and said fourth resistor and the other end of said fifth resistor electrically connected to a third terminal of said silicon control rectifier, wherein said intersection is said output terminal of said starting control circuit; and

a sixth resistor having one end electrically connected to said third
25 terminal of said silicon control rectifier and the other end electrically connected to said microprocessor.

7. The surge protection and reset circuit according to claim 6, wherein

said starting control circuit further comprises a buffer and inverting circuit mounted between said microprocessor and said sixth resistor for increasing a fan-out current and providing a trigger signal to said third terminal of said silicon control rectifier.

5 8. The surge protection and reset circuit according to claim 7, wherein said buffer and inverting circuit comprises:

a seventh resistor having one end electrically connected to said output terminal of said microprocessor;

10 a second transistor having a base terminal electrically connected to the other end of said seventh resistor and a collector terminal electrically connected to said sixth resistor;

a ninth resistor having one end electrically connected to an emitter terminal of said second transistor and the other end electrically connected to a voltage supply; and

15 an eighth resistor having one end electrically connected to a collector terminal of said second transistor and the other end electrically connected to ground.

9. The surge protection and reset circuit according to claim 1, wherein said surge protection and reset circuit further comprises a second voltage regulator having a control terminal electrically connected to said lamp-state terminal of said ballast and having an output terminal electrically connected to an application-specific integrated circuit (ASIC) for providing a second voltage level to said application-specific integrated circuit when said lamp-state terminal of said ballast outputs
20 said lamp-state signal to said control terminal of said second voltage
25 regulator.

10. The surge protection and reset circuit according to claim 9, wherein

said surge protection and reset circuit further comprises:

an OR gate logic circuit having two input terminals electrically connected to said application-specific integrated circuit (ASIC) respectively and said output terminal of said starting control circuit;

5 a third voltage regulator having a control terminal electrically connected to an output terminal of said OR gate logic circuit for providing a third voltage level when said third voltage regulator receives a signal from said OR gate logic circuit; and

10 a fan electrically connected to an output terminal of said third voltage regulator for dissipating heat of said surge protection and reset circuit when said fan receives said third voltage level.

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